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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/642,458
Filing Date: August 18, 2000
Appellant(s): MACINNIS ET AL.

Mirut P. Dalal
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/26/2006 appealing from the Office action mailed 12/12/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,909,559	So	6-1999
6,466,581	Yee	10-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The final rejection finally rejected claims 1, 5, 6, 9-11, 14-17, 20-22, 24, 26, 27, 30-32, 35, 36, 39, 41, 50, 51, and 53 and 54 under 35 USC 102 as being anticipated by So, U.S. Patent No. 5,909,559, finally rejected claim 15 as being obvious over So, U.S. Patent No. 5,909,559, and finally rejected claims 2, 3, 7, 8, 12, 13, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38, and 49 over So, U.S. Patent No. 5,909,559, in view of Yee et al., U.S. Patent No. 6,466,581. These rejections are reproduced below for the Board's convenience.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 6, 9-11, 14-17, 20-22, 24, 26, 27, 30-32, 35, 36, 39, 41, 50, 51, and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by So, U.S. Patent No. 5,909,559.

So teaches integrating a north bridge with a MPEG coder decoder (compression decompression) at column 133 lines 47-67. This section of the patent states:

Chip 510 has its memory size and pinout tailored for 3D graphics and geometry slope/setup, MPEG compression/ decompression algorithms, and/or 3D audio. Advantageously, CPU 315 is relieved of burden of much of these calculations, and freed from much time-consuming MMX context switching latency. Another embodiment of chip 510 integrates blocks 520 and 525 together with advantageously low real estate and reduced pinout, and PCI/PCI block 530 is a separate chip.

In FIG. 6, another embodiment 600 of an improved computer system is comparable to FIG. 5 except that a north bridge-type block 610 has a first VSP core enhancing the north bridge PCI/MCU circuitry and that first VSP runs 3D geometry and multimedia extensions acceleration. A second VSP block 620 virtualizes 3D audio, graphics, slope/setup and MPEG audio/video compression/decompression. Blocks 610 and 620 are integrated together into a single integrated circuit chip, and both blocks 610 and 620 are coupled to PCI bus 330 as master/slave agents. An accelerator bus 615 couples blocks 610 and 620. PCI/PCI bridge 530 is on or off-chip in different embodiments.

Claim 1:

So teaches a system on a single integrated circuit chip (*column 133 lines 29-67*) comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams (*So teaches applying the integration of the Northbridge and MPEG decompression and compression algorithms to a set-top box which to one of ordinary skill in the art is connected to broadcast cable which by applicants definition MPEG broadcast is MPEG Transport. The only function associated with this processor is receiving which is a broad process met by So's chip receiving the MPEG Transport stream.*), at least one of the MPEG Transport streams including MPEG video data (*Column 133 line 62.*);

an MPEG video decoder for decoding the MPEG video data to generate video using an external memory for displaying (*Column 133 lines 29-67, especially note line*

62 which specifically discusses MPEP video decompression which is MPEG decoding. An external memory is used for displaying the generated video.);

a display engine (graphics elements 126, 315, 345, 350, 510, 520, 525, 620) for processing graphics to be blended (*This is an intended function but not an actual function because blending is actually not occurring.*) with the video using the external memory (*Applicant needs to more concretely claim the elements of 1400 as illustrated in figure 40.*); and

a system bridge controller having a north bridge function disposed between a CPU (*CPU 315*) and a plurality peripheral devices (*Devices listed in block 550 (1394, TV, LAN, WAN, ATM), devices connected to south bridge 410, and any devices connected to PCI buses 330 and 540.*) for coupling the CPU to the plurality of peripheral devices (*Column 133 lines 29-67, especially note lines 57-58 which discuss north bridge type block 610 which performs north bridge function.*),

wherein the MPEG video decoder , the display engine, and the system bridge controller are implemented on the single integrated circuit chip (*Column 133 lines 29-67, note especially lines 33-38 and 63-65.*), and

wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip (*Figures 5 and 6 and column 133 lines 29-67 clearly teach the CPU and the peripheral devices are external to the integrated circuit 510 shown in figure 5 and integrated circuit chip containing 610 and 630. column 133 lines 41-45 clearly discuses 550 to be separate chips from the chip containing the north bridge and MPEG video decoder.*), and

wherein the external memory has a unified memory architecture (*Column 16 lines 62-63 and column 99 lines 58-67 discuss unified memory as the memory for the whole system, CPU, MPEG decoding, and graphics.*), such that the external memory is concurrently used by the CPU through the system bridge controller as at least a part of its main memory (*This is interpreted to mean also all of its main memory.*), the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data.

Claim 41:

So teaches a system on a single integrated circuit chip (*column 133 lines 29-67*) comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams (*So teaches applying the integration of the Northbridge and MPEG decompression and compression algorithms to a set-top box which to one of ordinary skill in the art is connected to broadcast cable which by applicants definition MPEG broadcast is MPEG Transport. The only function associated with this processor is receiving which is a broad process met by So's chip receiving the MPEG Transport stream.*), at least one of the MPEG Transport streams including MPEG video data (*Column 133 line 62.*);

an MPEG video decoder for processing MPEG video data to generate video for displaying (*Column 133 lines 29-67, especially not line 62 which specifically discusses MPEP video decompression which is MPEG decoding.*); and

a system bridge controller having a north bridge function disposed between a CPU (CPU 315) and a plurality peripheral devices (*Devices listed in block 550 (1394, TV, LAN, WAN, ATM), devices connected to south bridge 410, and any devices connected to PCI buses 330 and 540.*) for coupling the CPU to at least one of the MPEG Transport processor and the MPEG video decoder, and to the plurality of peripheral devices (*Column 133 lines 29-67, especially note lines 57-58 which discuss north bridge type block 610 which performs north bridge function.*),

wherein the MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip (*Column 133 lines 29-67, note especially lines 33-38 and 63-65. The set-top box inherently contains MPEG Transport processor and MPEG video decoder.*), and

wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip (*Figures 5 and 6 and column 133 lines 29-67 clearly teach the CPU and the peripheral devices are external to the integrated circuit 510 shown in figure 5 and integrated circuit chip containing 610 and 630. Column 133 lines 41-45 clearly discuses 550 to be separate chips from the chip containing the north bridge and MPEG video decoder.*).

This system claim adds to system claim 1 "an MPEG Transport processor for receiving a plurality of MPEG transport streams, at least one of the MPEG Transport streams including MPEG video data". So discusses two MPEG streams, audio and video, see

column 133 line 62. Thus, a transport processor is in the MPEG coder/decoder to allow both streams to be processed.

Claim 5:

Column 133 lines 29-67 discusses the north bridge connecting the CU to the PCI peripheral devices.

Claim 6:

Inherently PCI bus master allows one PCI device to communicate to another PCI device without using CPU as an intermediate device.

Claim 9:

The 550 and 560 are an I/O devices.

Claim 10:

The north bridge 520, 610 allows DMA between CPU 315 and memory 325.

Claim 11:

The north bridge 520 is connected to memory 525 and to any memory connected to the PCI bus.

Claim 14:

The single integrated circuit 510, 610 has a north bridge block 520 that connects the CPU to the MPEG video decoder 525, 620.

Claim 15:

Column 126 line 55 discusses MIPS processor.

Claim 16:

Column 100 lines 34-35 discusses burst in PCI.

Claim 17:

The north bridge inherently has buffers to buffer speed contention between differing devices.

Claim 20:

HDTV means high definition TV which is inferred by referenced to television at column 129 line 31.

Claim 21:

SDTV means standard definition TV which is NTSC TV, PAL TV, and SECAM TV which is discussed at column 129 line 57.

Claim 50:

This claim depends upon claim 9. So discusses attaching an ISA bus along with the PCI bus. The ISA bus (8 bits or 16 bits) has less bits than the PCI bus (32 bits or 64 bits), thus, the north bridge converts CPU data of 32 or 64 bits to ISA bus data of 8 or 16 bits.

Claim 53:

Column 157 line 55 to column 158 line 13 discusses integrating all of the components except for CPU and memory onto a single integrated circuit. This application is directed to multimedia and web applications thus it teaches compositing graphics and MPEG and since it has a single integrated circuit teaching the patent teaches to one of ordinary skill in the art this claim.

Claim 54:

This application implements DirectX function in VSP hardware, VSPs 525 and 620 are external to the CPU 315, and DirectX has a DirectX Blend function. Column 34 line 61 to column 36 line 62 discusses implementing DirectX in hardware to relieve the CPU of graphics processing such as the DirectX Blend function.

Claim 22:

This claims a method claim version of system claim 41 and it is rejected for the reasons given for claim 1 above.

Claim 24:

Both figures 5 and 6 illustrate the north bridge of the single integrated circuit chip communicating between the CPU and the rest of the chip's internal components such as 525, 620.

Claim 26:

This claims a method claim version of system claim 5 and it is rejected for the reasons given for claim 5 above.

Claim 27:

This claims a method claim version of system claim 6 and it is rejected for the reasons given for claim 6 above.

Claim 30:

This claims a method claim version of system claim 9 and it is rejected for the reasons given for claim 9 above.

Claim 31:

This claims a method claim version of system claim 10 and it is rejected for the reasons given for claim 10 above.

Claim 32:

This claims a method claim version of system claim 11 and it is rejected for the reasons given for claim 11 above.

Claim 35:

This claims a method claim version of system claim 16 and it is rejected for the reasons given for claim 16 above.

Claim 36:

This claims a method claim version of system claim 17 and it is rejected for the reasons given for claim 17 above.

Claim 39:

This claims a method claim version of system claim 20 and it is rejected for the reasons given for claim 20 above.

Claim 51:

This claims a method claim version of system claim 50 and it is rejected for the reasons given for claim 50 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over So, U.S. Patent No. 5,909,559. Column 126 line 55 discusses MIPS processor but does not specifically mention SH3 processor and SH 4 processor. These two processors are SuperH RISC microprocessors from Hitachi. The MIPS microprocessor is another RISC microprocessor but from Silicon Graphics. It would have been obvious to one of ordinary skill in the art to substitute one well known RISC microprocessor for another RISC microprocessor since they have similar capabilities, thus, the selection of which RISC microprocessor can be based upon economics at any one point in time.

Claims 2, 3, 7, 8, 12, 13, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over So, U.S. Patent No. 5,909,559, in view of Yee et al., U.S. Patent No. 6,466,581.

These claims claim big endian and little endian. Before analyzing these claims it is important to define these terms which may be found in An Essay on Endian Order.

Copyright (C) Dr. William T. Verts, April 19, 1996.

Little endian definition:
"Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. (The little end comes first.)
Intel processors (those used in PC's) use "Little Endian" byte order.
Big endian definition:
"Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address. (The big end comes first.)
Motorola processors (those used in Mac's) use "Big Endian" byte order.
The essay may be found at http://www.cs.umass.edu/~verts/cs32/endian.html

Another useful definition teaching a system that uses either type is from webopedia:

Many mainframe computers, particularly IBM mainframes, use a big-endian architecture. Most modern computers, including PCs, use the little-endian system. The PowerPC system is *bi-endian* because it can understand both systems
This definition may be found at http://www.webopedia.com/TERM/b/big_endian.html

Yee at column 4 lines 30-48 and column 7 lines 33-48, teach converting from little endian to big endian and from big endian to little endian at a PCI controller in order to allow a PowerPC to have access to peripheral devices such as a memory using different endian.

It would have been obvious to one of ordinary skill in the art at the time of applicants invention to incorporate little endian to big endian and from big endian to little endian conversion in the chip carrying the north gate function because this will allow the CPU to interface with diverse peripheral devices that do not use the same endian as the CPU.

(10) Response to Argument

Appellant presents separate arguments for each grouping of claims: claim 1 at pages 10-13; claims 41, 2, 3, 5-21, 49, 53, and 54 at pages 14-17; claim 20 at pages 17-18; and claims 22-39 at pages 18-21. The arguments presented for independent claims 1, 41, and 22 are substantially the same, however, it should be noted that claims 41 and 22 do not claim the argued display engine, thus, this portion of appellants' argument is not considered pertinent to these claims. The following response to the arguments follows the headings used by appellant after a general discussion of So.

So teaches virtualizing many major hardware elements onto a single Northbridge die, refer to column 18 lines 15-34:

The VSP wrapper is not redundant to the audio, MIDI or graphics interface because it replaces and permits virtualization of major hardware elements that have to be purchased today. The VSP wrapper (and even the VSP as a whole i.e. wrapper/DSP) offers modular circuitry available to integrate essentially for free on the spare die (or spare gates) real estate that hitherto have existed in the I/O bound and bond-pad-limited North Bridge and South Bridge chips.

VSPs provide plenty of DSP MIPS to differentiate new designs from those based only on the main microprocessor i.e. host CPU. For example, a 233 MHz Klamath processor with 2 instructions/cycle may offer 400-500 host MIPS and can do 30 frames/sec DVD decoding (AC-3 audio and MPEG-2 video) entirely in software. Hardware assists for Klamath (and other host CPUs) at I/O locations are, however, needed. The VSP approach not only provides these hardware assists but also leverages DSP MIPS to do more than the same number of host MIPS can do. This leveraging can be measured in raw MIPS, effective MIPS, and bandwidth reduction.

So teaches partitioning system functionality into single-chip solutions, refer to column 130 lines 53-55:

Different embodiments partition system functionality into respective single-chip solutions which can have the same type of package as the MPU 106, such as plastic package.

So teaches integrating the CPU and Northbridge into a single chip, refer to column 132 lines 23-37:

In FIG. 3, an improved computer system embodiment for telecom, audio, networking, and 3D graphics has CPU 315 and improved north bridge 318 integrated into a single chip 310. North bridge 318 is coupled to main memory 325, and with CPU 315, also to a cache 320. A north bridge includes PCI bus bridge and memory controller circuitry such as found in an Intel north bridge or is improved as shown and described, for instance, in connection with incorporated patent application TI-18329 FIG. 11 depicting a chip 103 with description in many figures and text therein. North bridge 318 has improved circuits therein such as shown in FIGS. 22, 126 and 127 and has a host CPU either integrated thereon or provided as a separate chip. PCI bus 330 corresponds to PCI bus 124 of FIG. 1.

So teaches integrating the Northbridge 520 and MPEG compression/decompression 525 onto a single chip 510, refer to column 133 lines 29-55 noting lines 47-55:

Chip 510 has integrated on a single chip a north bridge 520 coupled by an accelerator bus 515 to a VSP core 525. VSP core 525 has a VSP-improved integrated circuitry incorporating the DSP 1730 and wrapper 1720 circuitry of FIG. 50 and runs VSP Kernel software according to USP shared memory model. Chip 345 also includes PCI master/slave coupling to PCI bus 330. Additionally, a PCI/PCI bridge 530 couples between VSP core 525 and interfaces to a secondary PCI bus 540. A chip or chips 550 couple to PCI bus 540 and provide 1394 serial bus, TV, LAN (local area networking), WAN (wide area networking) and ATM (asynchronous transfer mode, broadband ISDN integrated services digital network) and RF interface 560.

Chip 510 has its memory size and pinout tailored for 3D graphics and geometry slope/setup, MPEG compression/ decompression algorithms, and/or 3D audio. Advantageously, CPU 315 is relieved of burden of much of these calculations, and freed from much time-consuming MMX context switching latency. Another embodiment of chip 510 integrates blocks 520 and 525 together with advantageously low real estate and reduced pinout, and PCI/PCI block 530 is a separate chip.

Claim 1

A So does teach "an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data"

The arguments concerning "MPEG transport processor" and "MPEG transport stream" have been considered, but, since the So reference discusses using the single chip in set-top boxes which are used to receive cable broadcasts then So teaches using a MPEG transport processor to process MPEG transport steams received by the set-top box in the single integrated chip 510 that receives and decompresses MPEG data streams. So discusses set-top box and television set at column 3 lines 35-38 and 58-61, column 129 lines 22-31, and column 134 lines 48-51 and discusses receiving cable broadcast at column 130 lines 33-40. Claim 1 does not claim the function of the transport processor other than "for receiving a plurality of transport streams", therefore, a processor that receives the MPEG data transport stream for further processing of the MPEG transport stream meets this broad claim limitation. Appellants' specification does not give a clear definition for the claim term "MPEG transport processor", see figures 40 and 41 which illustrates three processors 1600, 1602 and 1614 each with different functions regarding the MPEG transport data stream and page 129 line 6 to page 130 line 20 and page 149 line 1 to page 152 line 4 which describes the different functions which includes receiving the MPEG transport stream to be used in the decompression process. Thus, one of ordinary skill in the art would associate with the set-top box of So

the ability to receive MPEG transport streams in the single chip 510 and especially associating receiving the MPEG transport streams for subsequent decompression purposes. Thus, to one of ordinary skill in the art the MPEG decompression associated with the single chip embodiment of So teaches the single chip will at least receive the claimed MPEG Transport streams which is taught by So to be both video and audio streams.

B So's teaching of a "Set Top Box" includes an MPEG Transport Processor as discussed above and So teaches that MPEG Transport Processor would be included on the single integrated circuit that also comprises "the MPEG Video Decoder", "display engine", and "system bridge controller".

The arguments concerning "MPEG transport processor" being included with "the MPEG Video Decoder", "display engine", and "system bridge controller" is not persuasive because chip 510 includes: 1) "MPEG transport processor" as discussed above; 2) "the MPEG Video Decoder", which decompresses the MPEG video transport see appellants specification at page 130 line 22 to page 131 line 17 and page 152 line 5 to page 154 line 35 and see So at column 133 lines 47-50 and; 3) "display engine", which processes graphics see So at column 133 lines 47-50; and 4) "system bridge controller", see So at column 133 lines 33-35.

Claims 41, 2, 3, 5-21, 49, 53, AND 54

A So does teach "an MPEG Transport processor for receiving a plurality of MPEP Transport streams, at least one of the MPEG Transport streams including MPEG video data"

The arguments presented under this heading on pages 15 and 16 of the Appeal Brief are substantially identical to the arguments present under heading A on pages 11 and 12 of the Appeal Brief, thus, these arguments are not persuasive for the same reasons given above for claim 1 under heading A.

B So's teaching of a "Set Top Box" includes an MPEG Transport Processor as discussed above and So teaches that MPEG Transport Processor would be included on the single integrated circuit that also comprises "the MPEG Video Decoder", "display engine", and "system bridge controller".

Claim 41 does not claim a display engine, thus, this portion of appellants argument is not considered pertinent to this claim.

The arguments presented under this heading on pages 16 and 17 of the Appeal Brief are substantially identical to the arguments present under heading B on pages 12 and 13 of the Appeal Brief, thus, these arguments are not persuasive for the same reasons given above for claim 1 under heading B.

Claim 20.

Appellants arguments concerning claim 20 at pages 17-18 of the Appeal Brief are not persuasive because So teaches at column 129 line 31 a television set which includes HDTV because the term television includes many television standards including HDTV. In the argument appellant states "the Examiner is attempting the logical fallacy of anticipating a species by the disclosure of its genus". This argument is incorrect because MPEP 2132.02 Rev. 5, Aug. 2006 states a species (HDTV) is anticipated by its genus (television) when one of ordinary skill in the art "at once envisage" the species from the genus. Since television includes many television standards including HDTV then one of ordinary skill in the art at once envisages HDTV in the teaching of So.

Claims 22-39

A So does teach "receiving a plurality of MPEG Transport streams using an MPEG Transport processor implemented on the integrated circuit chip, at least one of the MPEG Transport streams including MPEG video data"

The arguments presented under this heading on pages 19-21 of the Appeal Brief are substantially identical to the arguments present under heading A on pages 11 and 12 of the Appeal Brief, thus, these arguments are not persuasive for the same reasons given above for claim 1 under heading A.

B So's teaching of a "Set Top Box" includes an MPEG Transport Processor as discussed above and So teaches that MPEG Transport Processor would be included on the single integrated circuit that also comprises "the MPEG Video Decoder", "display engine", and "system bridge controller".

Claim 22 does not claim a display engine, thus, this portion of appellants argument is not considered pertinent to this claim.

The arguments presented under this heading on page 21 of the Appeal Brief are substantially identical to the arguments present under heading B on pages 12 and 13 of the Appeal Brief, thus, these arguments are not persuasive for the same reasons given above for claim 1 under heading B.

Appellant has provided no separate arguments concerning the second issue for review, see pages 9, 14, and 18 of the Appeal Brief, thus, dependent claims 2, 3, 7, 8, 12, 13, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38 and 49 remain rejected under 35 USC 103 and this rejection should stand or fall based upon appellants argument given for independent claims 22 and 41.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

It is assumed that appellant meant to include in both of the evidence appendix and the related proceedings appendix the statement of "NONE". See MPEP 1205.03 at page 1200-17 Rev. 3, August 2006.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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